ABSTRACT OF THE DISCLOSURE

Address translation control (ATC) limits the mappings between virtual and physical addresses in order to implement a memory access policy. Each processor in a multi-processor system maintains a translation lookaside buffer (TLB) that caches mappings to speed translation of virtual addresses. Each processor also maintains a counter. Each time a processor's TLB is flushed, the processor's counter is incremented. When a link to a page is removed from an address translation map, the counter values for all of the processors are recorded. When that page is accessed by a processor, the recorded counter values are compared with the processor's current counter value to determine whether the processor's TLB has been flushed since the link to the page was removed from the map. An expensive TLB flush operation is delayed until needed, but still occurs early enough to prevent an invalid TLB entry from being used to violate the access policy.